UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,715	04/15/2004	Christopher J. Borrelli	X-1641-3 US	6763

24309   7590   07/30/2007

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER
SHIN, CHRISTOPHER B

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
07/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	**Applicant(s)**
Office Action Summary	10/824,715	BORRELLI ET AL.
	Examiner	**Art Unit**	
	Christopher B. Shin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>07 May 2007</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-31</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-31</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____.

        3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   The Amendment received May 7, 2007 has been entered and carefully

considered. Claims 1-31 are pending in the application.

Response to Arguments

2.   Applicant's arguments filed May 7, 2007 have been fully considered but they are

not persuasive. The examiner has modified the art rejection in response to the

arguments.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Fidler (US 2003/0172176) in view of Conner et al. (US 2004/0111537).

    a.   The Fidler reference teaches all of the limitations of the claimed limitations

    as follows:

Claims 25-31   Fidler et al. (figures 1-2 & accompanying description)
- A data communication system
    o System of figure 1
- A network transceiver for communicating data using a protocol
    o (14)
- A processor for executing a protocol stack associated with said protocol

- o (26)
- Memory circuitry
  - o (20)
- A DMA controller (DMAC) for controlling said memory circuitry
  - o (18, 32)
- A MAC, coupled to said DMAC by a streaming interface
  - o (16 & 32), coupled to (18) by (22)
- A transmit peripheral having a first interface configured to receive a communication sequence from said DMAC over said streaming interface, said received communication sequence having data read from said memory circuitry
  - o (18, 21, 23, 32), two separate channels are used to transfer data to and from a network (12), see also [0015], "data from the processor 26 that is intended to be sent (transmitted) to the network 12 is also stored in the RAM memory 20 prior to being read by DMA controller 18, see also [0018] "RAM memory 20 ... for storing data carried in a single data packet 34"
- A receive peripheral having a second streaming interface configured to transmit a communication sequence to said DMAC over said streaming interface, said transmitted communication sequence having data written from said memory circuitry
  - o (18, 21, 23, 32), two separate channels are used to transfer data to and from a network (12), see also [0015], "data from the processor 26 that is intended to be sent (transmitted) to the network 12 is also stored in the RAM memory 20 prior to being read by DMA controller 18, see also [0018] "RAM memory 20 ... for storing data carried in a single data packet 34"
- MAC circuitry configured to transmit said data read from said memory circuitry to said network transceiver and received said data to be written to said memory circuitry from said network transceiver
  - o Feature of (22, 32, 16)
- Said protocol comprises a Gigabit Ethernet protocol
  - o Obvious feature of Ethernet
- A bus bridge (DCR) configured to receive control data from said processor, said control data operative to control said MAC circuitry
  - o Feature (32), see also [0015] bottom
- Wherein said communication sequence received by said transmit peripheral and transmitted by said received peripheral comprises a header, a data section, and a footer section
  - o Figure 2
- Control logic for extracting control data from at least one of said header and said footer
  - o Feature of processing (34, 26, 48) by (10, 14, 16)

- Checksum computation logic for computing checksum data for said data read from said memory circuitry in response to said control data
  - Feature of processing (34, 46) by (10, 14, 16)
- Checksum computation logic for computing checksum data for said data to be written to said memory circuitry
  - Feature of processing (34, 46) by (10, 14, 16)
- Control logic for inserting first control data into said header and second control data into said footer
  - Feature of processing (34, 36, 48) by (10, 14, 16)

- FIFO memory for storing data
  - (22)
- DMA descriptor
  - Feature of (18) utilizing figures 3 –4, see also [0019]

b.   As for the claims 25-31, as can be seen from the Fidler reference teaches all the basic principles that are equivalent/analogous to the claimed invention; however, the Fidler does not expressly show identical details of the claimed invention. For example, the exact details of the DCR Bridge, logic for handling checksum data, header, footer, data section, control data, DMA controller/descriptor; however, such details are common knowledge in the art of Interface device utilizing DMA-MAC controllers. As evidence, Conner reference is one of the example teaches & utilizes DMA-MAC controller with more details of DMA with gigabit Ethernet media access network controller for more efficient data handling.

Since both the Fidler and Connor references are form the same field of endeavor, it would have been obvious at the time the invention wad made to one having ordinary skilled in the art to come up with the invention from Fidler and the Conner for the reasons stated above.

c. ·   As for broader apparatus claims 1-14, the teachings of the claims 25-31

are similarly applied.

d.   As for method claims 15-19 & 20-24, the teachings of the claims 25-31 are

similarly applied. The examiner has further explained the detailed teachings of claims

15 and 20 for better explanation in response to the applicant's arguments.

Claims 15 & 20   Fidler et al. (figures 1-2 & accompanying description)
- A method of communicating data between a network transceiver and memory
  circuitry
    o System of figure 1
- Transmitting/receiving, over a streaming interface, communication sequence to
  DMA controller configured to control said memory circuitry
    o (18, 21/23, 32), see also [0015], "data from the
      processor 26 that is intended to be sent (transmitted)
      to the network 12 is also stored in the RAM memory
      20 prior to being read by DMA controller 18, see also
      [0018] "RAM memory 20 ... for storing data carried in
      a single data packet 34"
- Said communication sequence having a header, a data section, and footer, said
  data section including data to be written to said memory circuitry
    o Figure 2
- Computing checksum data for said data to be written to said memory circuitry
    o Feature of processing (34, 46) by (10, 14, 16)
- Inserting/extracting first/second control data into said header/footer
    o [0016], "those in the art will recognize that the   ·
      information contained in the data packet 34 is driven
      by the standard associated with the network 12 to
      which the embedded system 10 is interfaced"

Conclusion

5.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher B. Shin whose telephone number is 571-272-4159. The examiner can normally be reached on 6:30-5:00 M,Tu,Th,F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Kindred Alford can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CHRISTOPHER SHIN
PRIMARY EXAMINER
OF 2181

July 20, 2007
cs